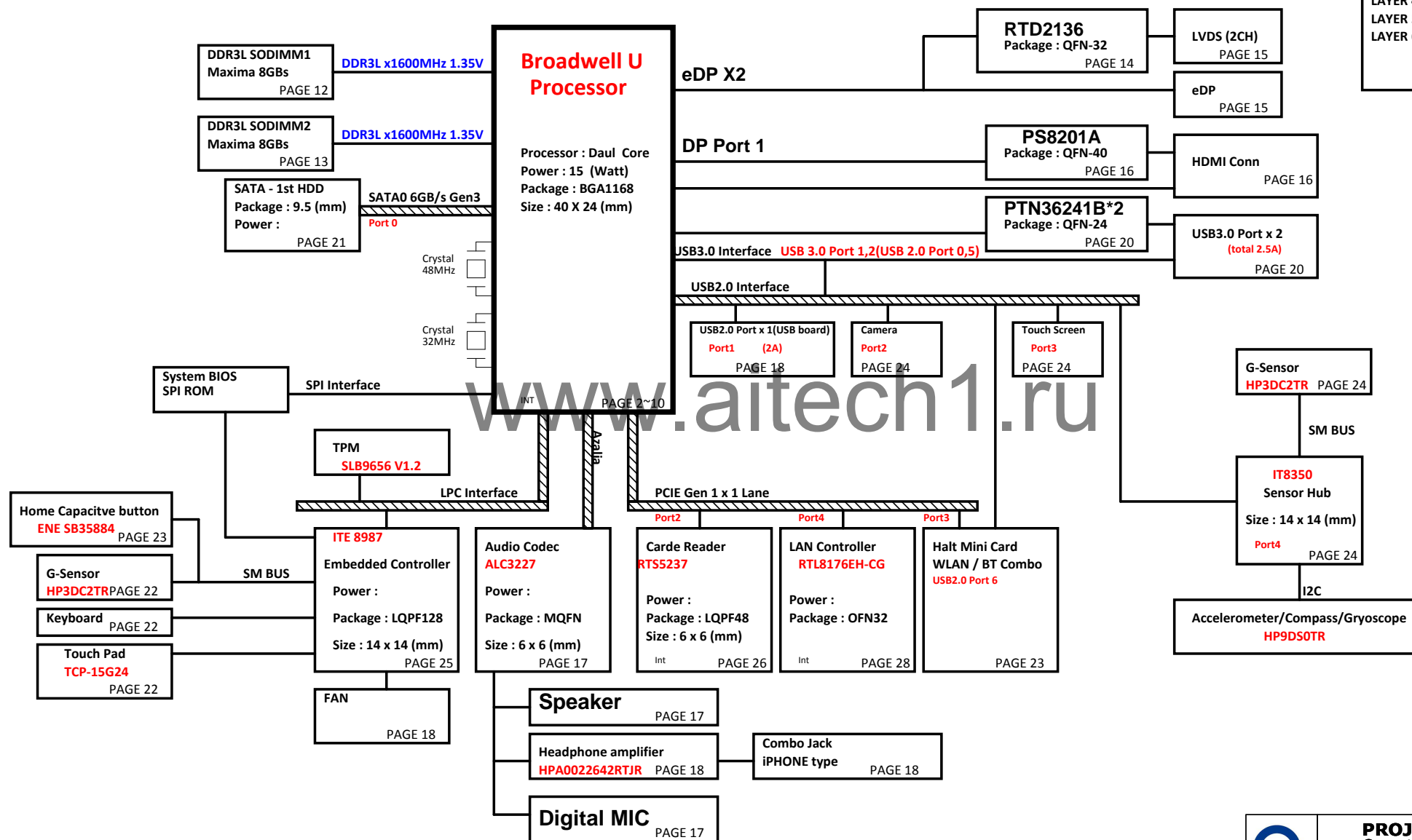


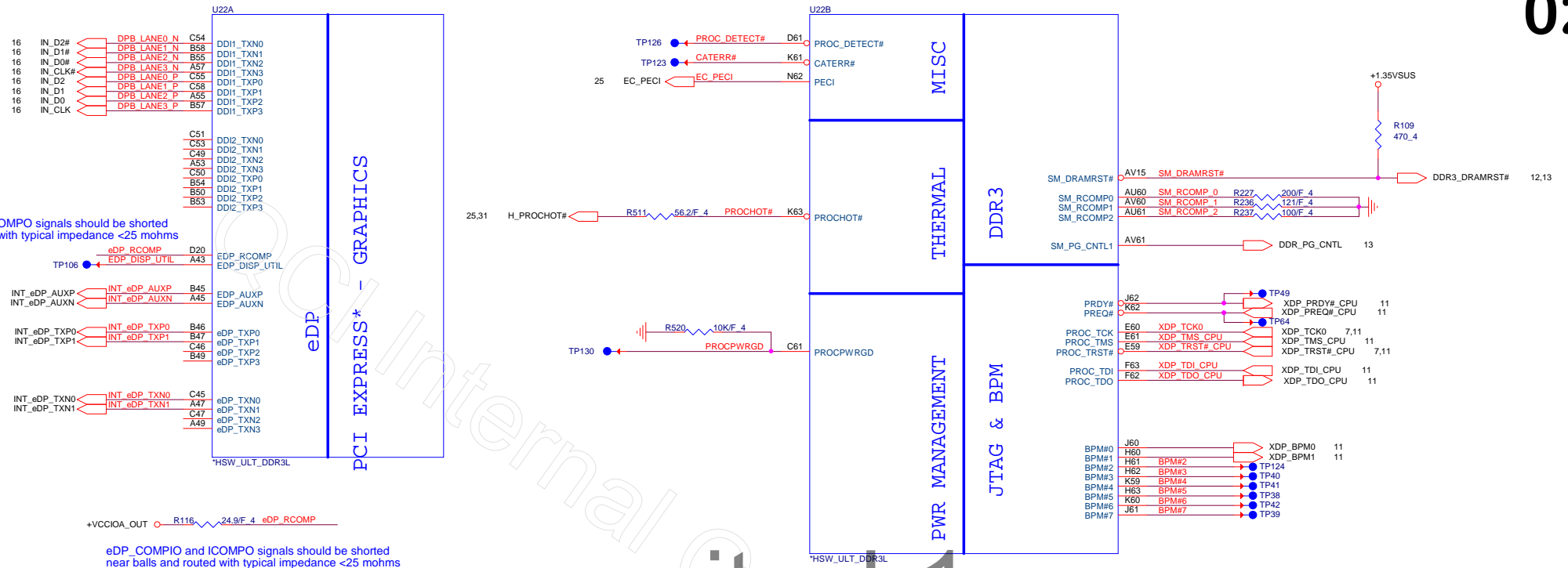
13"/15"

Y61 Intel Cresnet Bay ULT Platform Block Diagram

PCB 6L STACK UP

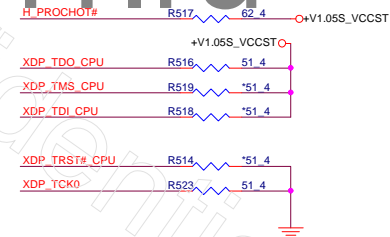
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT



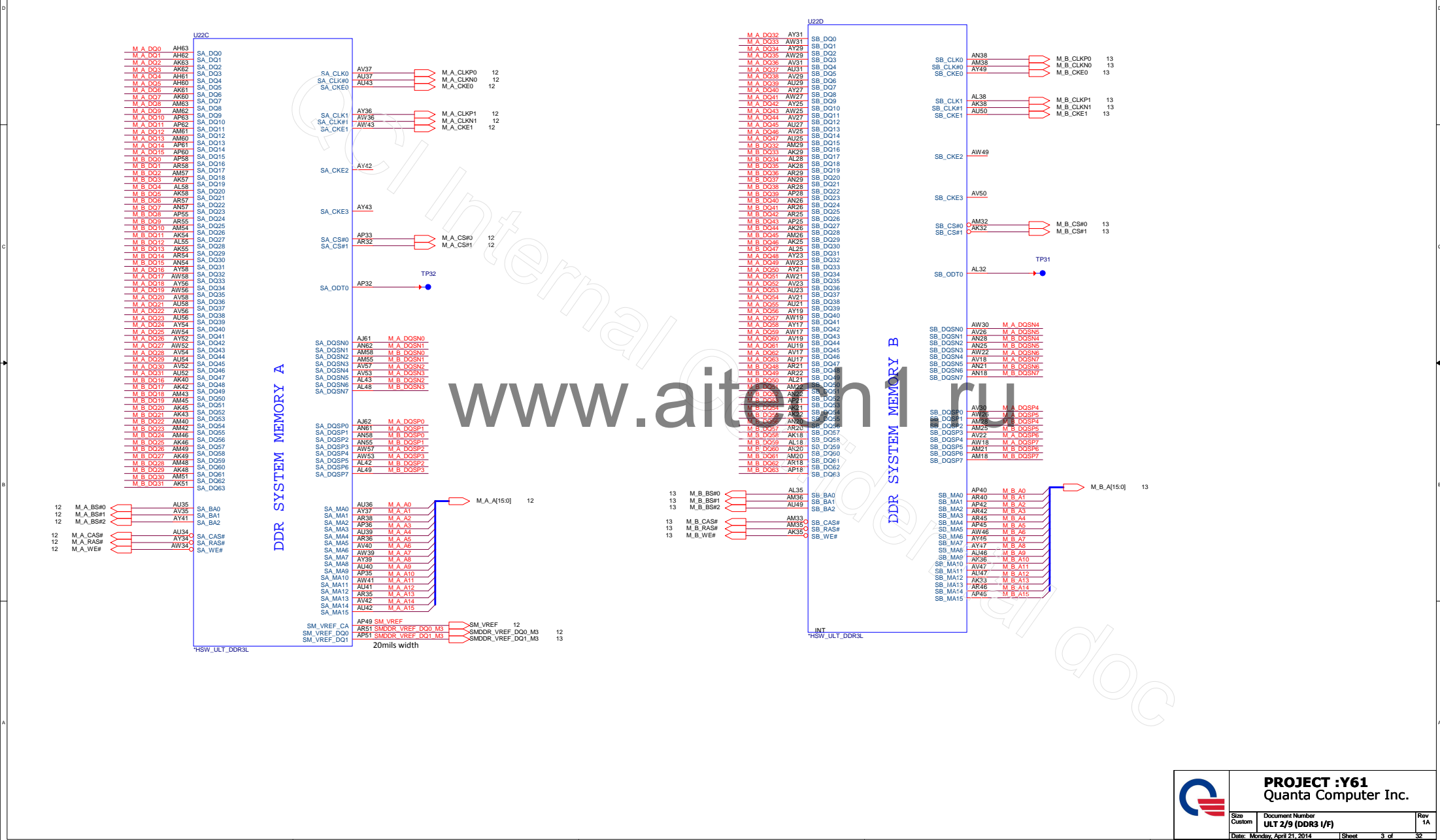


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Processor pull-up (CPU)

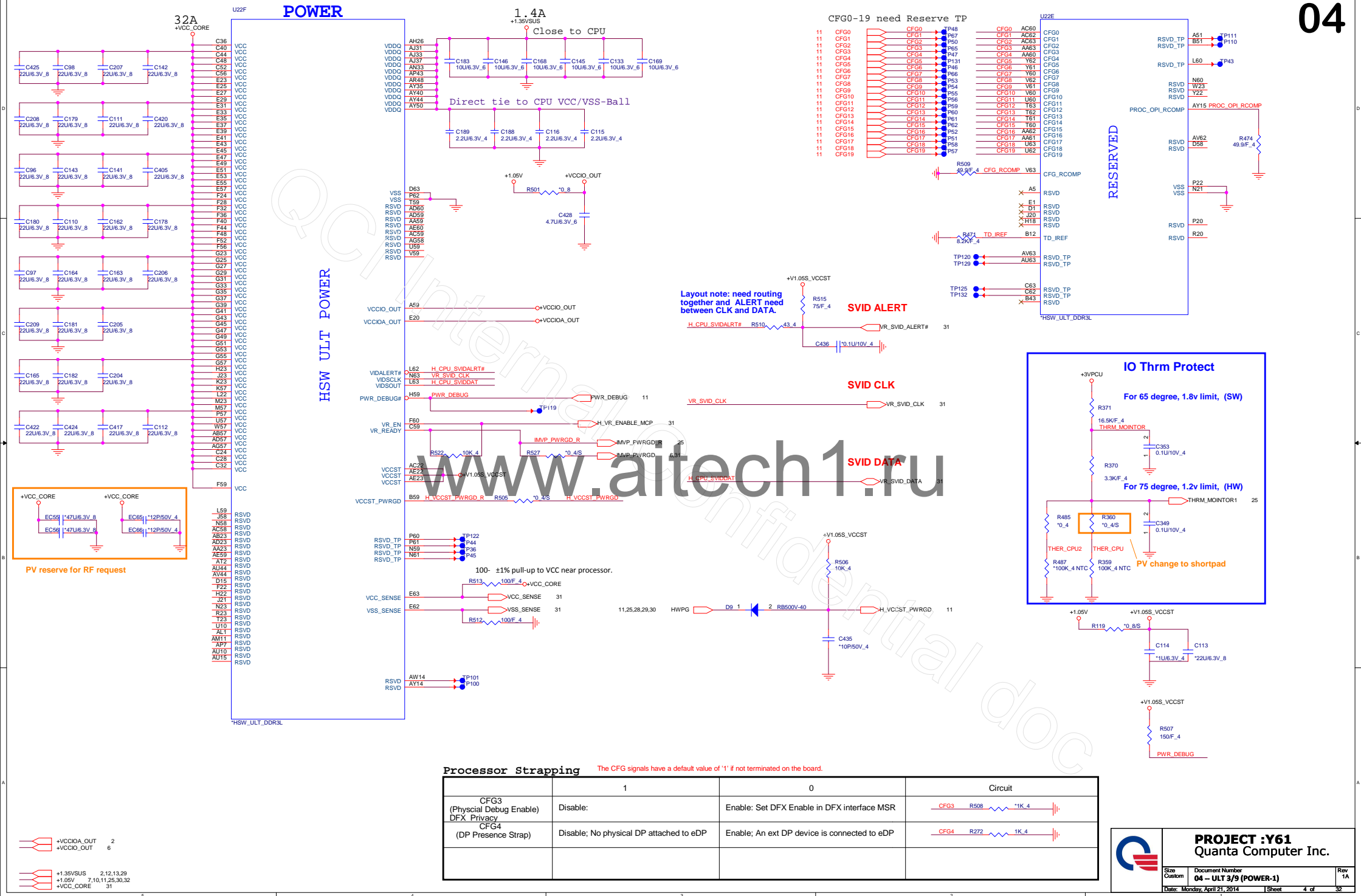


Haswell ULT Processor (DDR3L)



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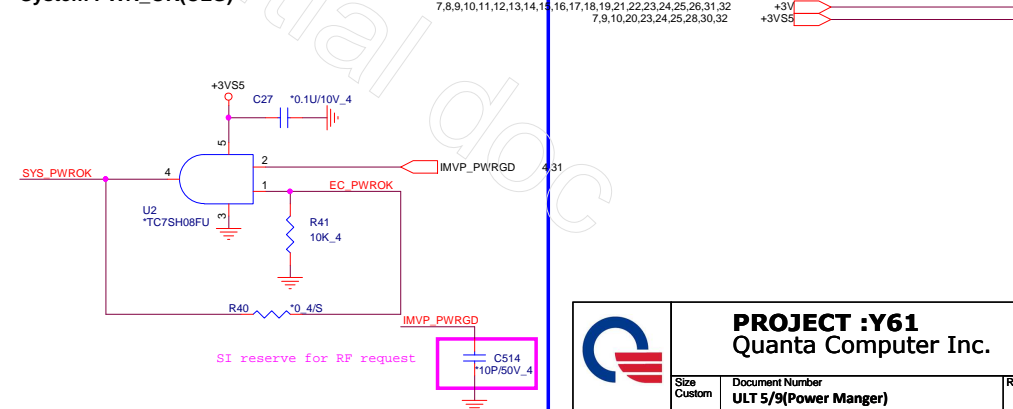
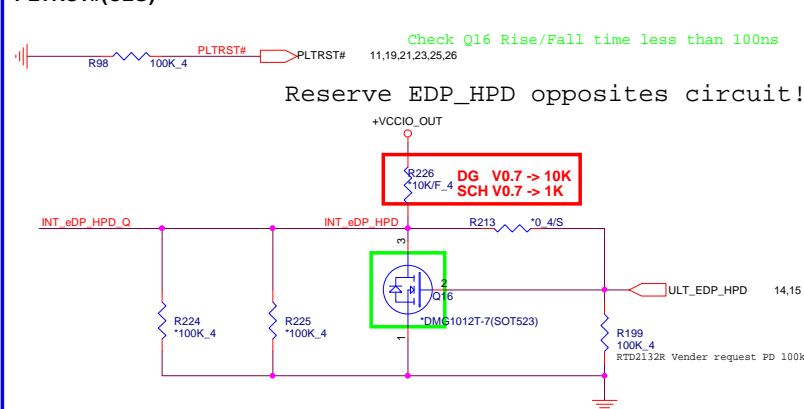
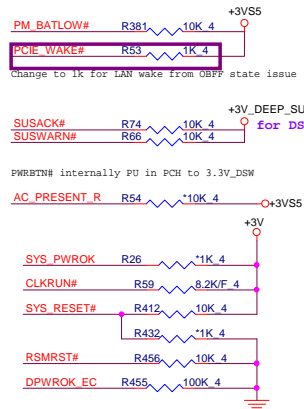
Size: Custom Document Number: ULT 2/9 (DDR3 I/F) Rev: 1A
Date: Monday, April 21, 2014 Sheet: 3 of 32



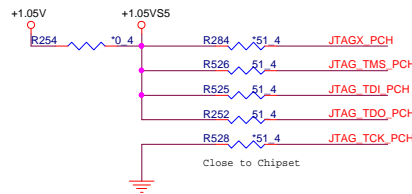




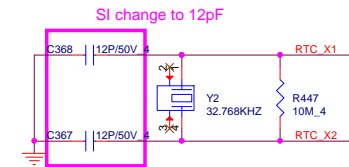
System PWR_OK(CLG)



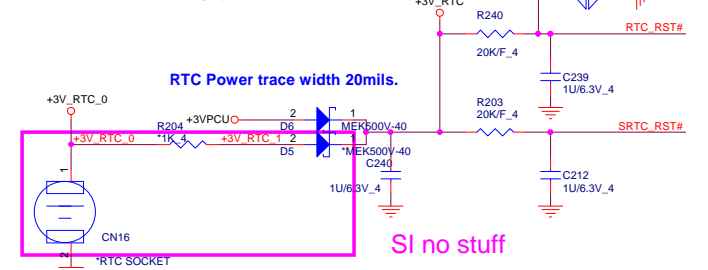
07



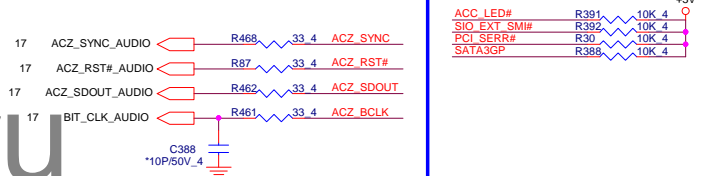
RTC Clock 32.768KHz



30mils

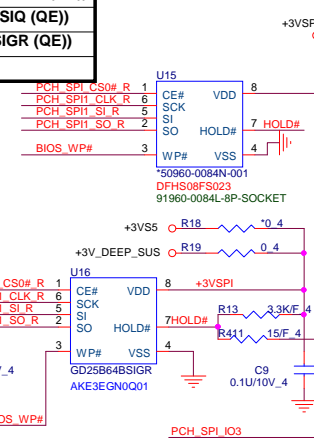


GPIO Pull UP

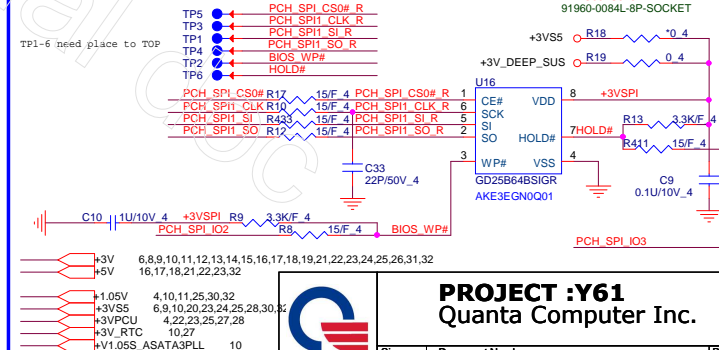


Vender	Size	P/N
EON	8MB	AKE3EZNOQ01 (EN25QH64-104HIP (QE
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ (QE))
GigaDevice	8MB	AKE3EGNOQ01 (GD25B64BSIGR (QE))
Socket		DFHS08FS023






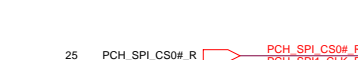

4M SPI ROM Socket



PCH SPI ROM(CLG)



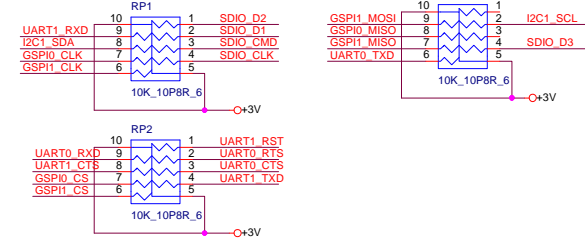
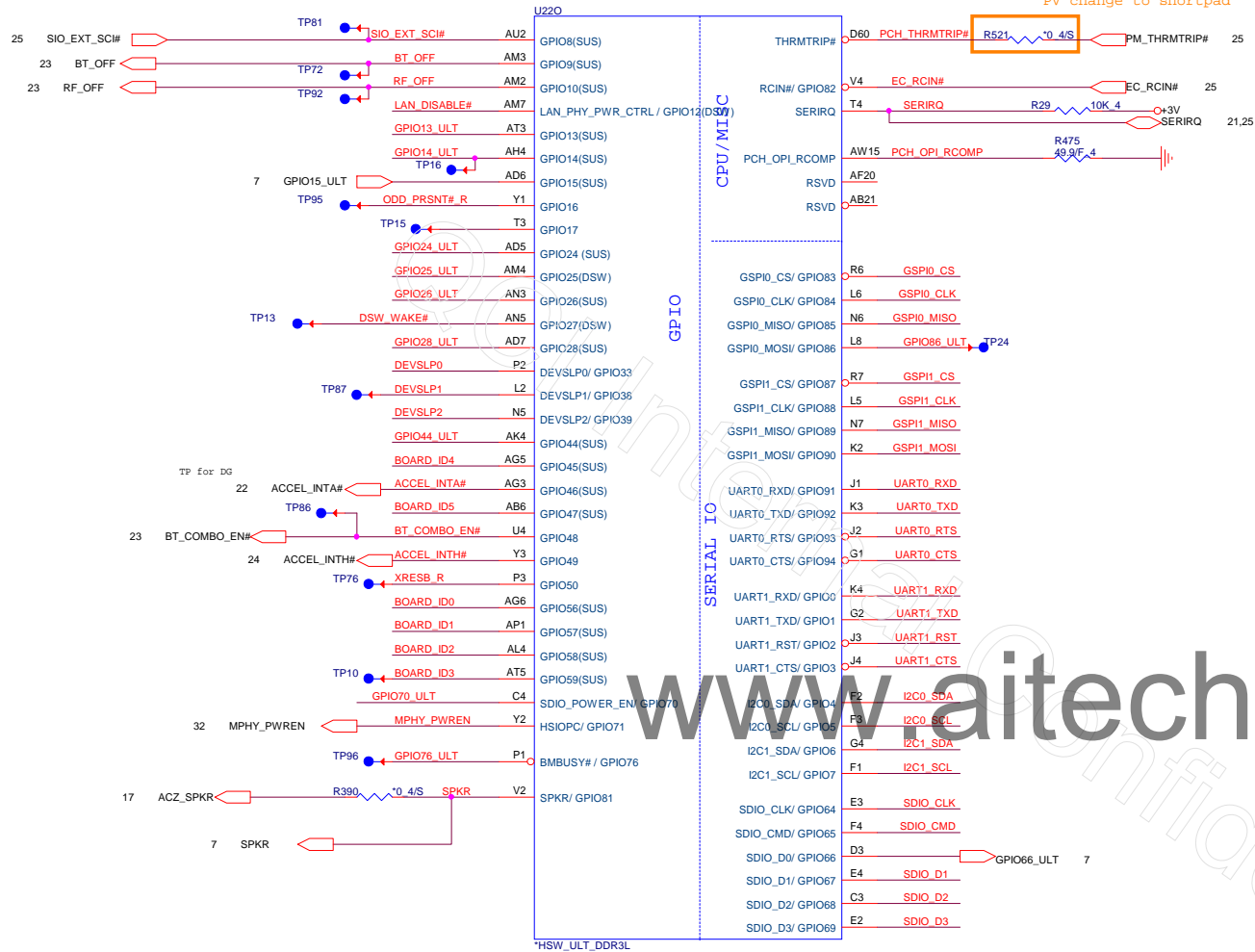
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up							
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overriden							
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	<table border="1" data-bbox="716 1136 909 1184"><tr><th>GNT0#</th><th>Boot Location</th></tr><tr><td>1</td><td>LPC</td></tr><tr><td>0</td><td>SPI(Default)</td></tr></table>	GNT0#	Boot Location	1	LPC	0	SPI(Default)	
GNT0#	Boot Location									
1	LPC									
0	SPI(Default)									
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality							
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up							
										

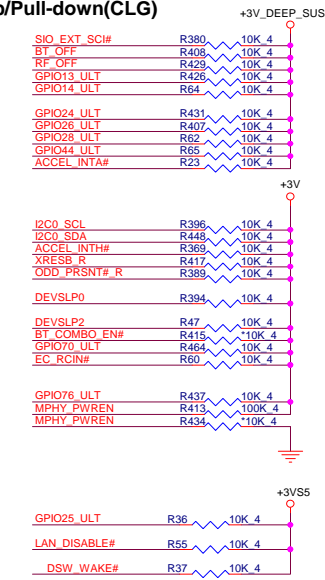
PROJECT :Y61
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Size Custom	Document Number ULT 6/9(SATA/HDA)	Rev 1A
Date: Monday, April 21, 2014		Sheet 7 of 32

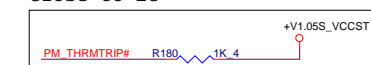
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA) Haswell (GPIO)



GPIO Pull-up/Pull-down(CLG)

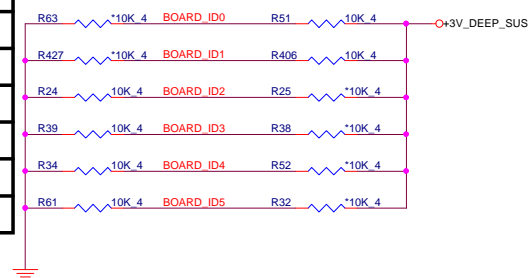


Close to EC



09

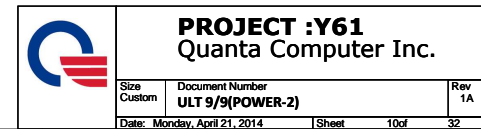
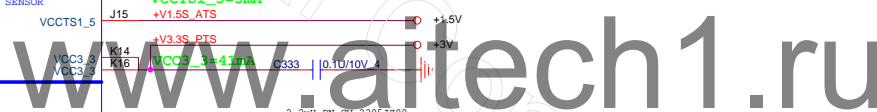
Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
13" clamshell wo/TS	0	0	0	0	0	1
13" convertible w/TS	0	0	0	0	1	0
15" convertible w/TS+ Giga NIC	0	0	0	0	1	1
13" clamshell w/TS (Reserve)	0	0	0	0	0	0
13" convertible wo/TS (Reserve)	0	0	0	0	0	0
15" convertible w/TS (Reserve)	0	0	0	0	0	0

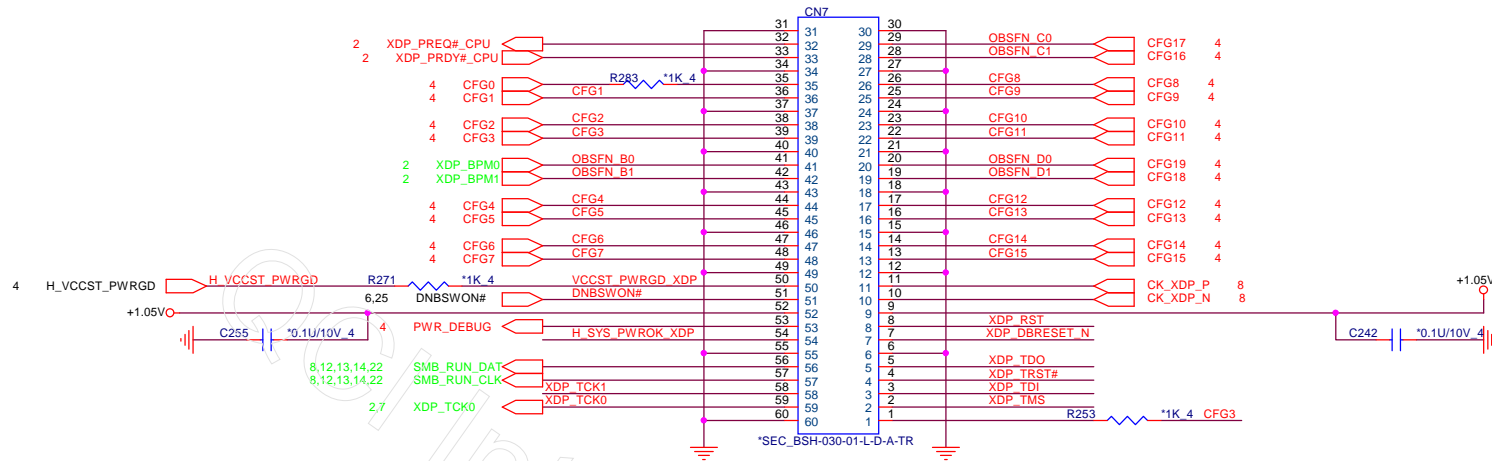


6,7,8,10,11,12,13,14,15,16,17,18,19,21,22,23,24,25,26,31,32
6,7,10,20,23,24,25,28,30,32

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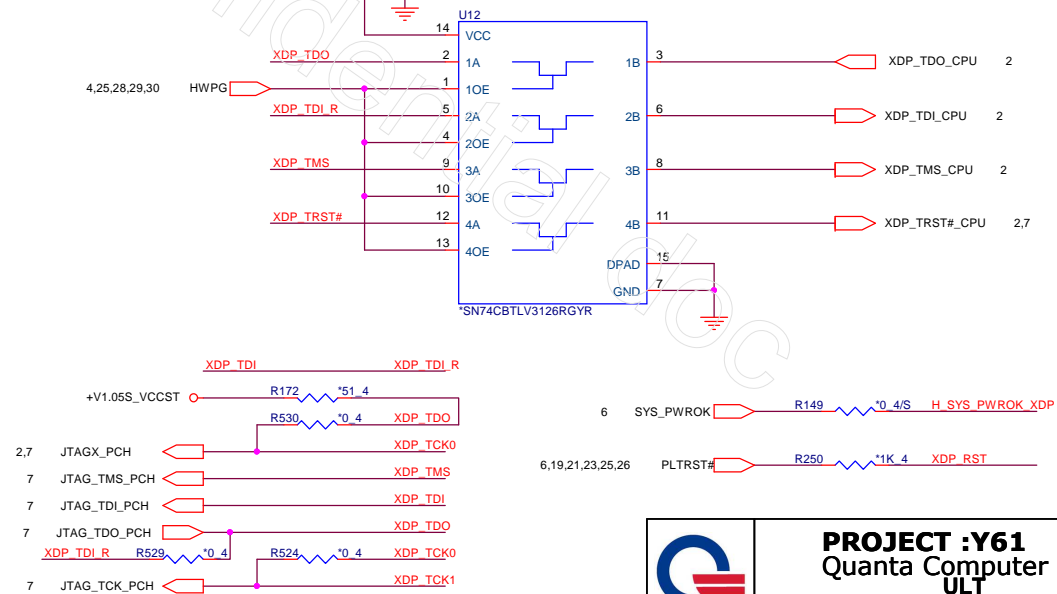
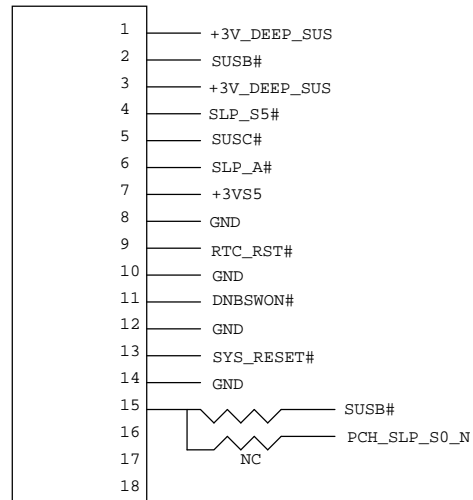
Size Custom	Document Number ULT 8/9 (GPIO/MISC)	Rev 1A
Date: Monday, April 21, 2014	Sheet	9 of 32



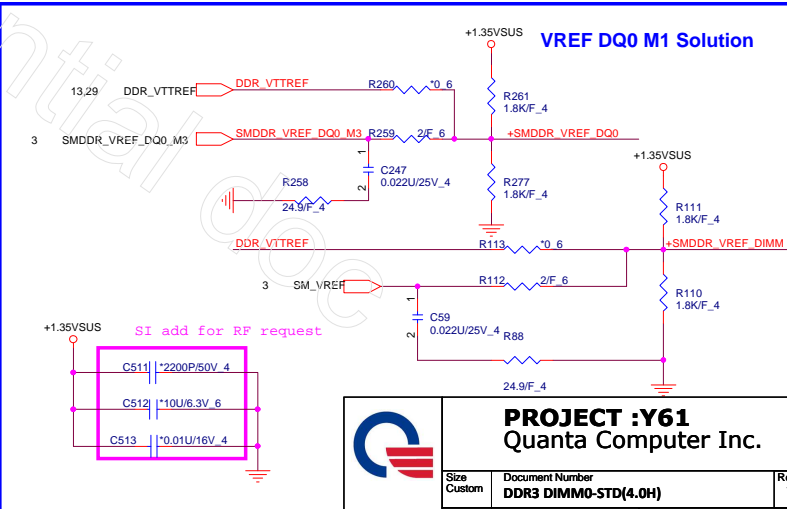
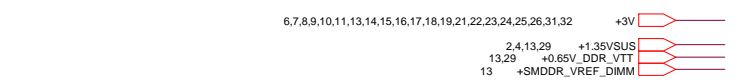


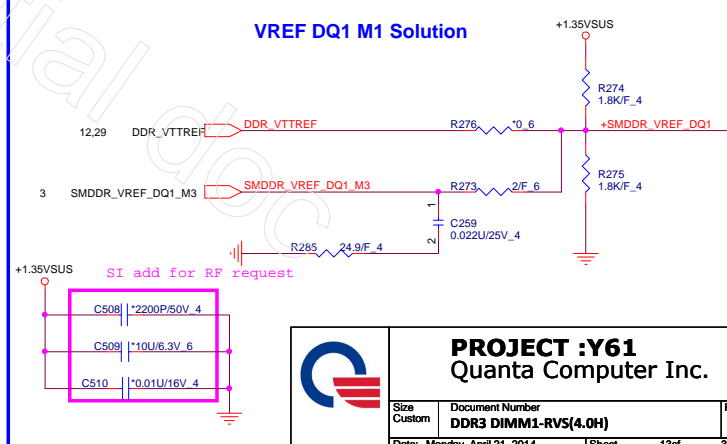
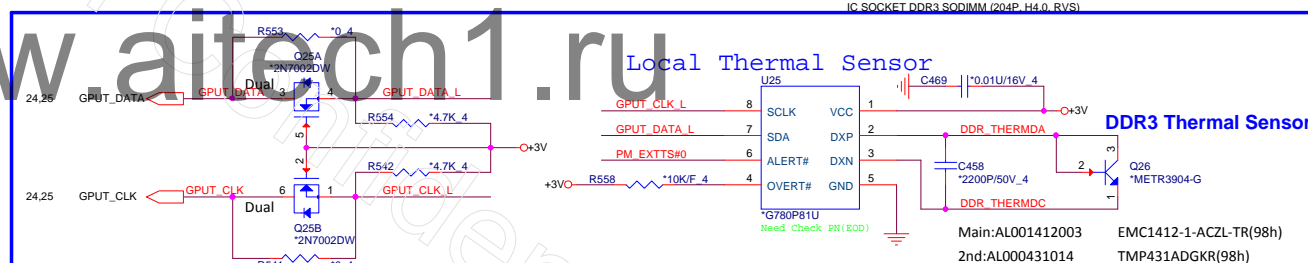
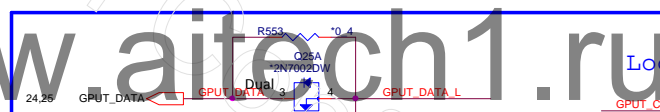
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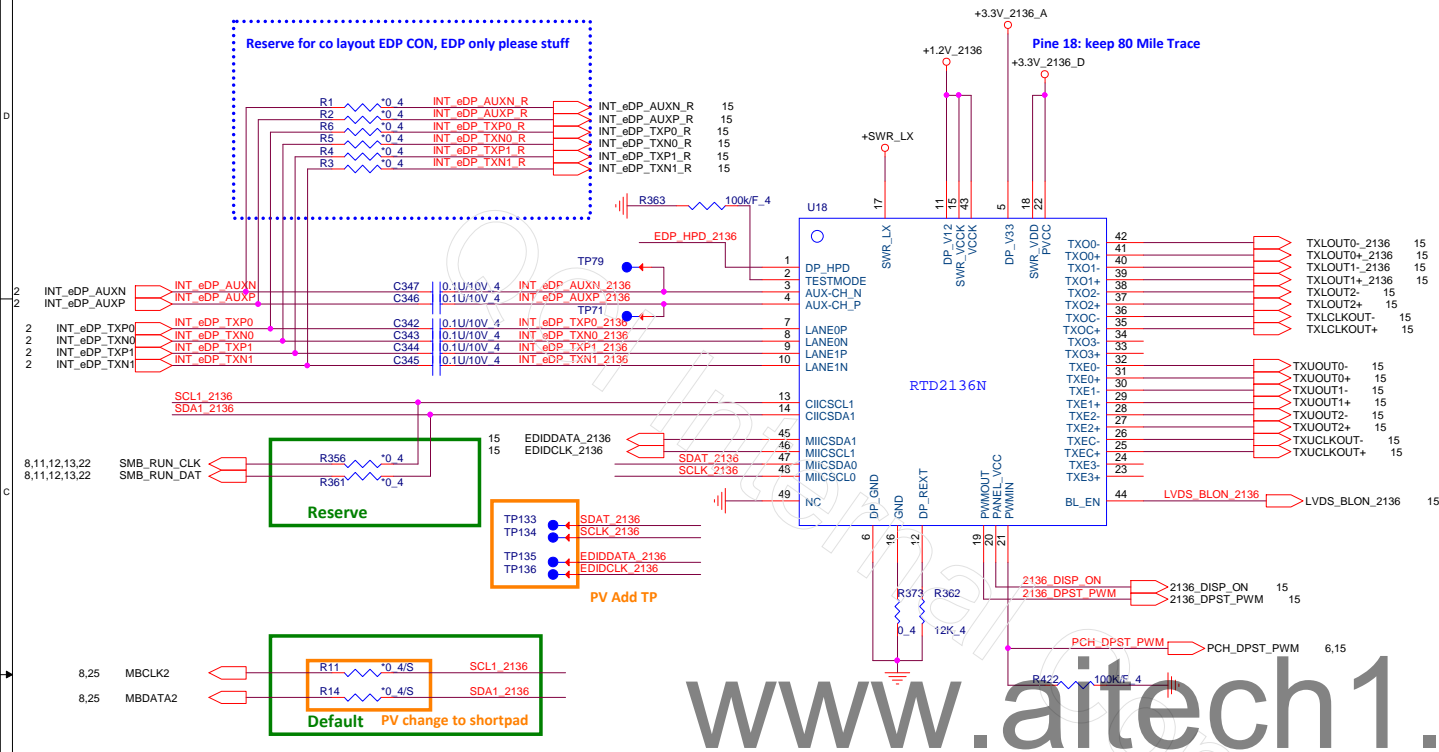
APS



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ULT





EDDID EEPROM
VCC

DP2LVDS VCC

HPD

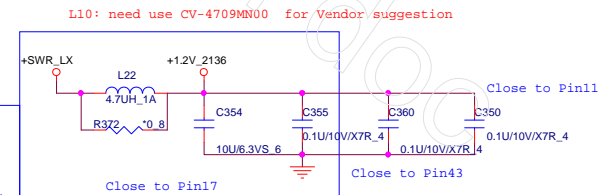
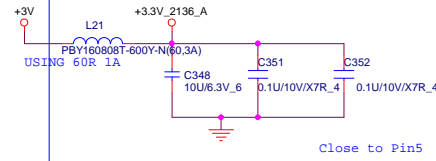
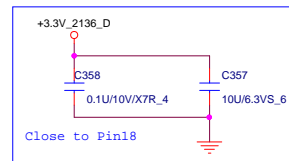
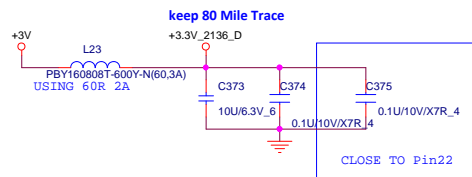
<=100ms

PV remove EEPROM

For EDP: unstuff Ra

Ra

6.15 ULT_EDP_HPDP



SWR MODE	LDO MODE
Stuff L22	Stuff R372

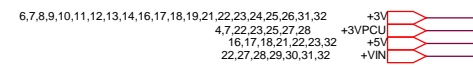
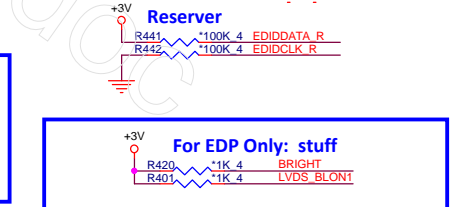
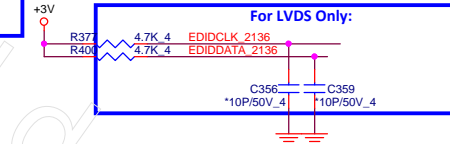
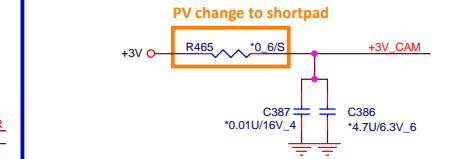
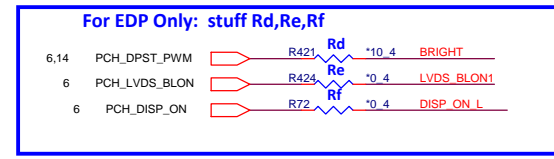
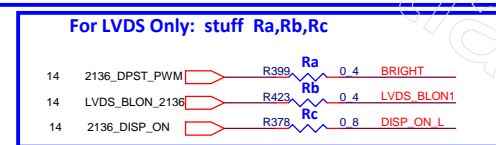
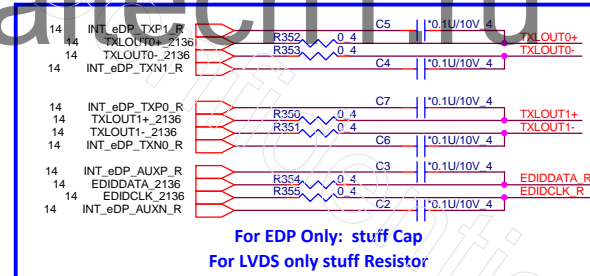
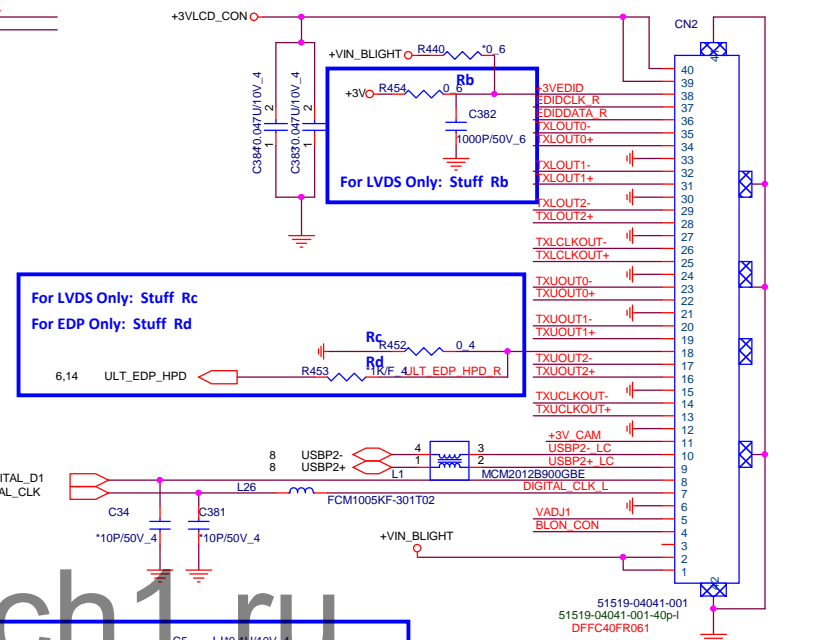
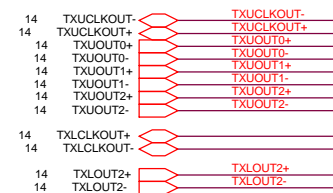
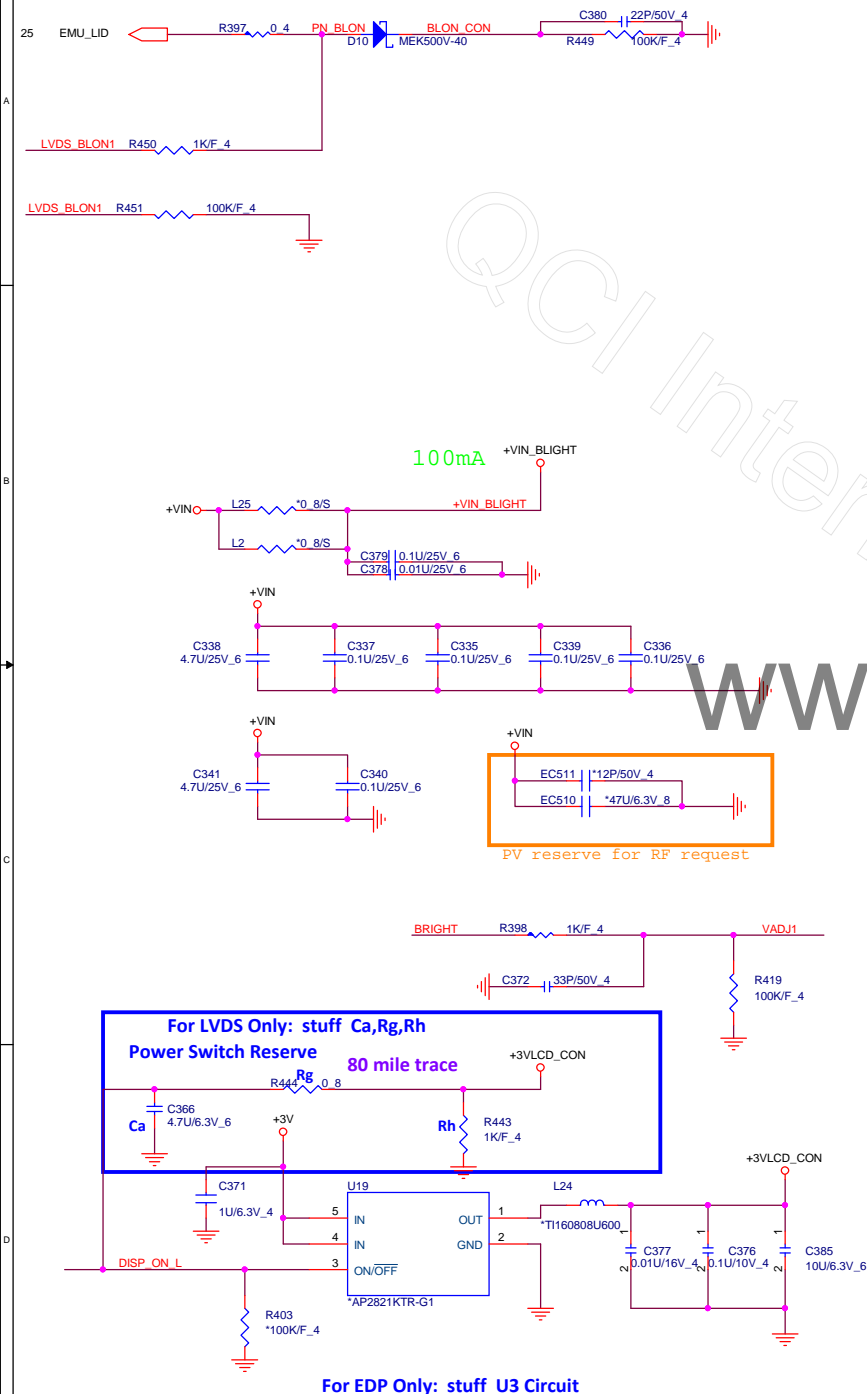
PROJECT :Y61
Quanta Computer Inc.

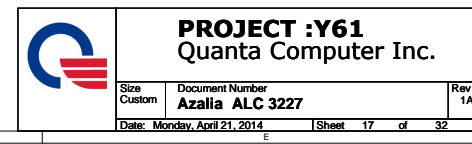
Size	Document Number	Rev
Custom	RTD2136	1A
Date: Monday, April 21, 2014	Sheet 14 of 32	

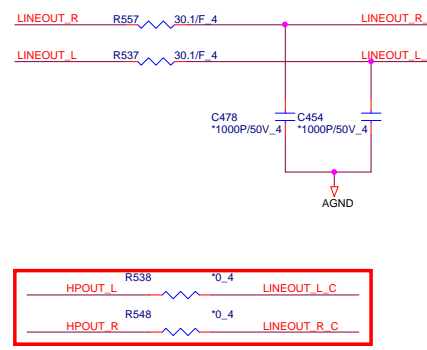
LID Switch

LVDS Conn.

15

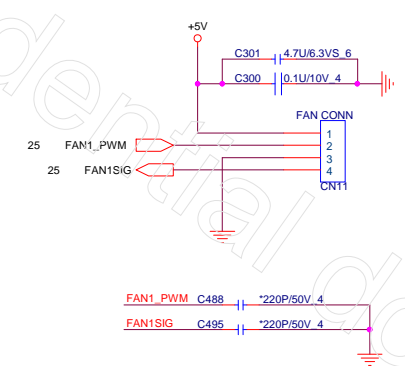







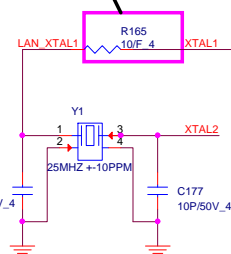
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FAN



	<h1>PROJECT :Y61</h1> <h2>Quanta Computer Inc.</h2>		
	Size Custom	Document Number	R
	Audio/AMP HPA022642RTJR		
Date: Monday, April 21, 2014		Sheet 18 of 32	

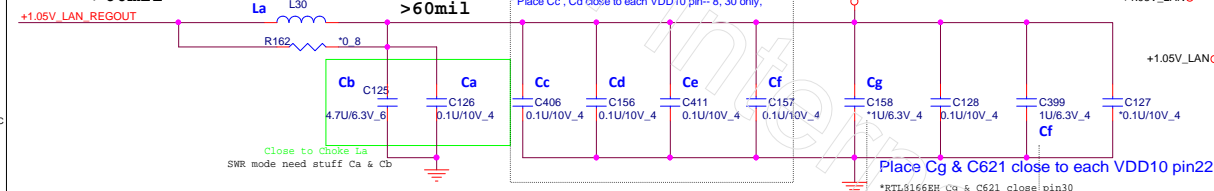
For EMI 0 ~ 22 ohm



```
Trace<30 mil
Width > 60 mil
      >60mil
```

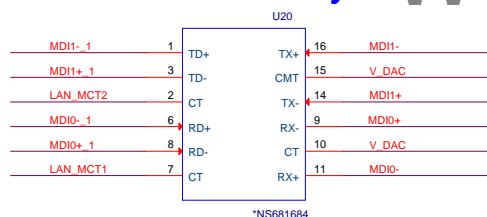
Power trace Layout 寬度> 60mil

>60mil



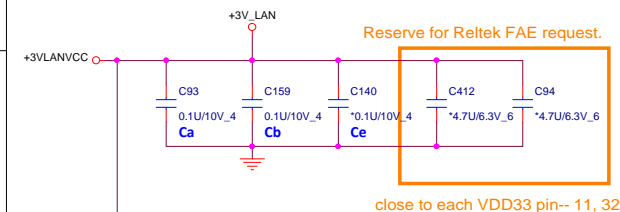
* Place Cg close to each VDD10 pin-- 22 (reserve)

10/100 only

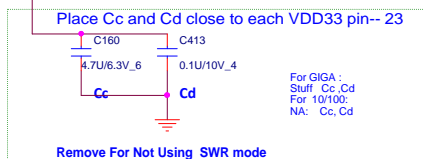


*NS681684

BOT: TST1284R LF DB0EL5LAN00



close to each VDD33 pin-- 11, 32



For GIGA :
 Stuff Cc, C
 For 10/100
 NA: Cc, C

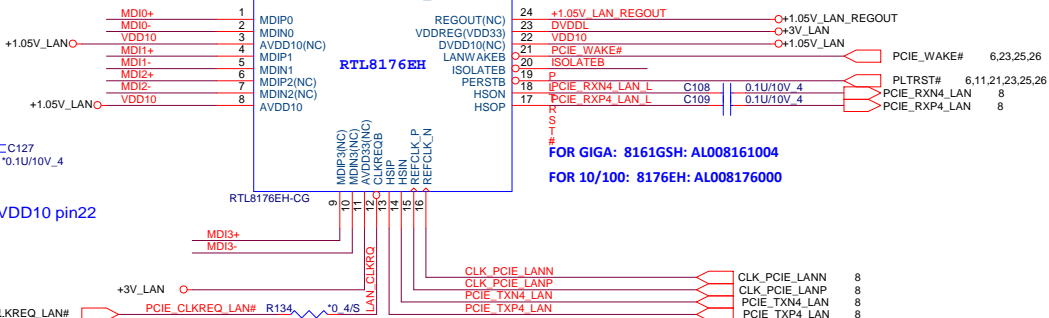
Remove For Not Using SWR mode

6,7,8,9,10,11,12,13,14,15,16,17,18,21,22,23,24,25,26,31,32

+3V

+3VLANVCC

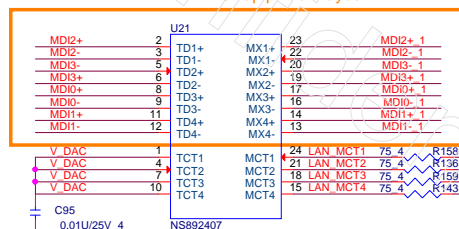
Please add 9 GND VIAs
connection with thermal PAD



FOR GIGA: 8161GSH: AL008161004
FOR 10/100: 8176EH: AL008176000

Giga only

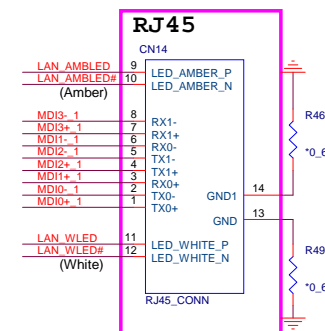
Swap pin for Layout



For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 .DB0LL1LAN00

For 10/100
BOT: TST1284R LF DBOEL5LAN00

LAN conn

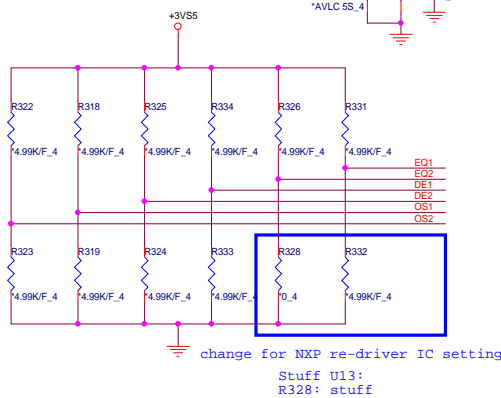
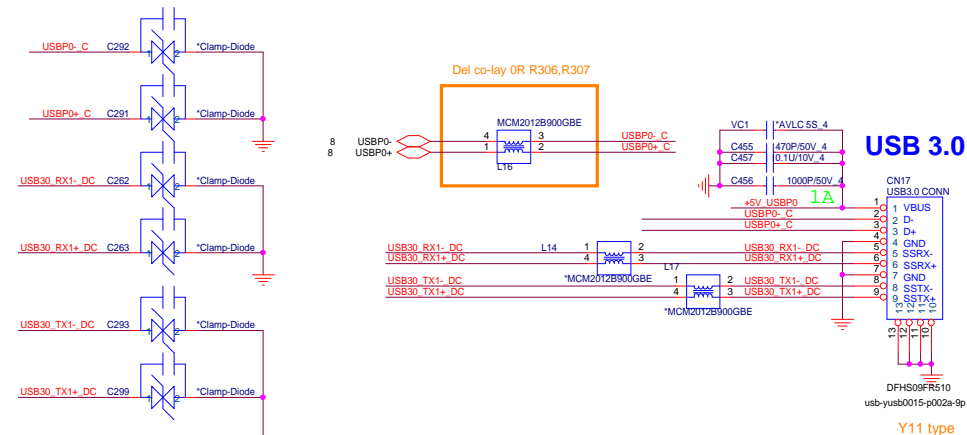
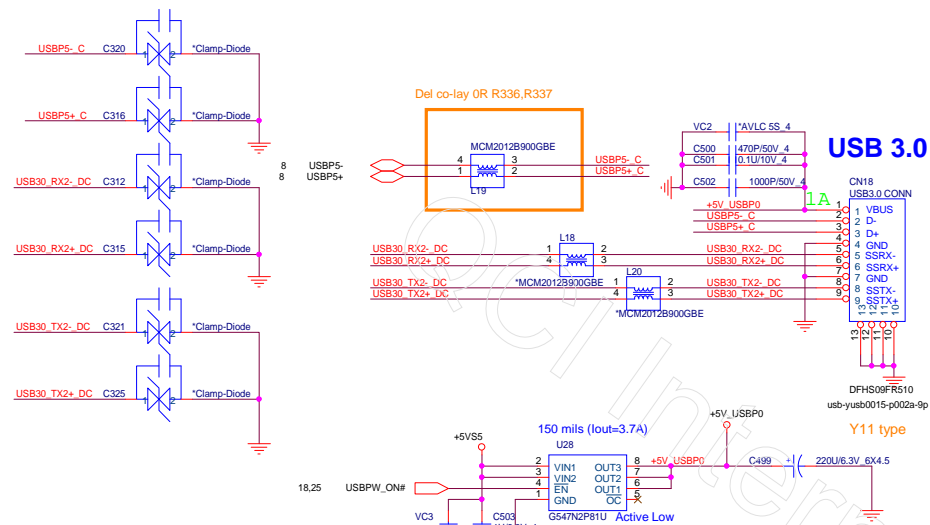


SI change footprint to
ri45-2ri3060-128111f-12p

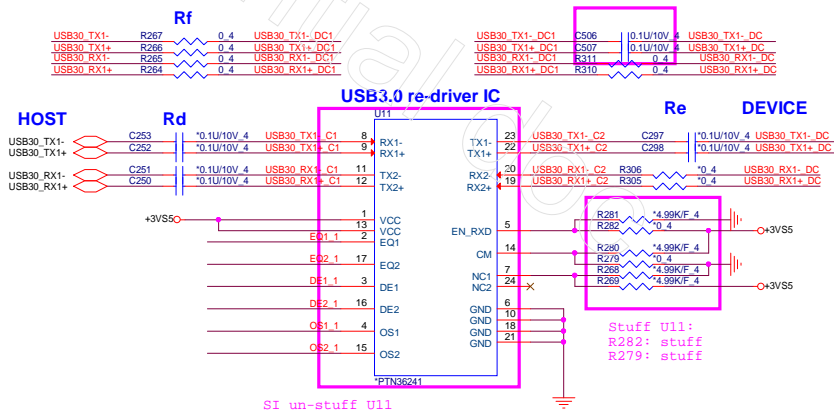
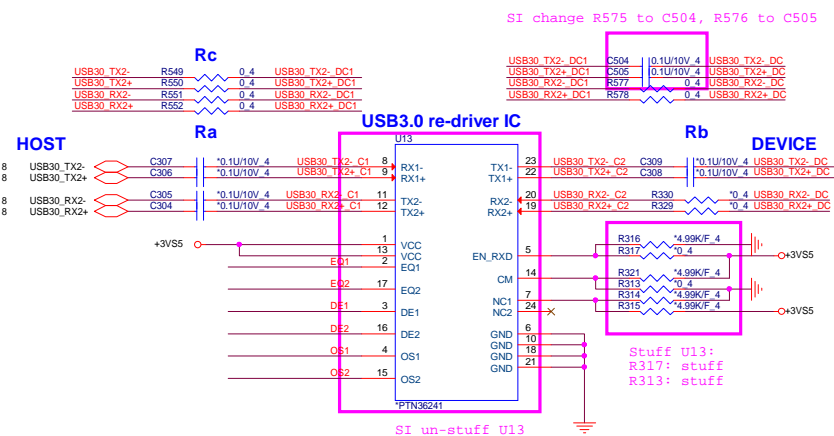
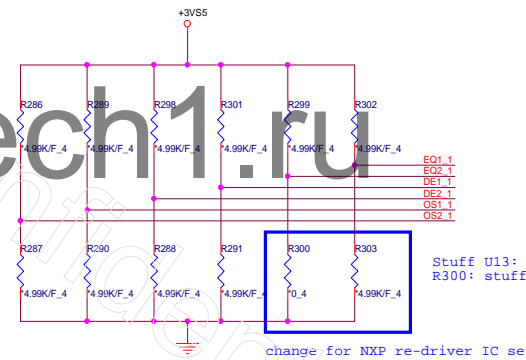


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OSx	Transition Bit Amplitude		
NC(default)	1000		
0	870		
1	1085		
EQx	Equalization dB		
NC(default)	0		
0	7		
1	15		
DEx	OSx=NC	OSx=0	OSx=1
NC	-3.5dB	-2.2dB	-4.4dB
0	-6.0dB	-5.2dB	-6.0dB
1	-8.5dB	-8.9dB	-7.6dB
EN_RXD	DEVICE FUNCTION		
1(default)	Normal operating mode		
0	Sleep mode		
CM	DEVICE FUNCTION		
0(default)	Normal operating mode		
1	Compliance mode		

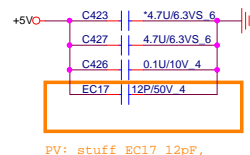
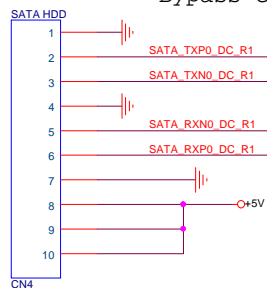


6,7,9,10,23,24,25,28,30,32
13,18,28,29,30,31,32
4,7,22,23,25,27,28

+3V55
+6V55
+3VPCU

SATA HDD Connector(Cable type)

Bypass CAP close conn



PV: stuff EC17 12pF,

SI add for co-lay use

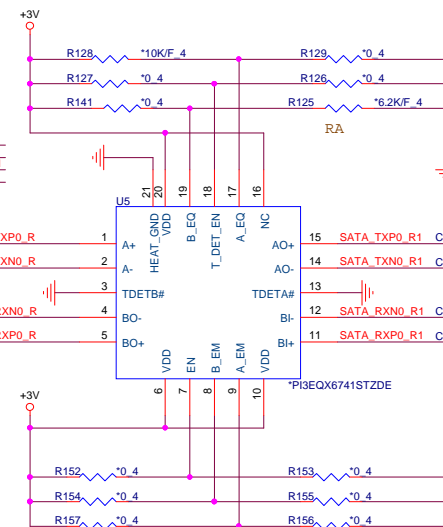
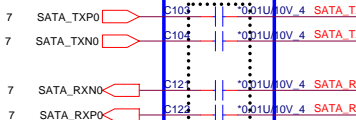
SATA_TXP0_DC_R1 R584 *0.4 SATA_TXP0_DC_R
SATA_TXN0_DC_R1 R586 *0.4 SATA_TXN0_DC_R
SATA_RXN0_DC_R1 R585 *0.4 SATA_RXN0_DC_R
SATA_RXP0_DC_R1 R587 *0.4 SATA_RXP0_DC_R

SATA_TXP0_DC_R2 R589 *0.4 SATA_TXP0_DC_R
SATA_TXN0_DC_R2 R591 *0.4 SATA_TXN0_DC_R
SATA_RXN0_DC_R2 R588 *0.4 SATA_RXN0_DC_R
SATA_RXP0_DC_R2 R590 *0.4 SATA_RXP0_DC_R

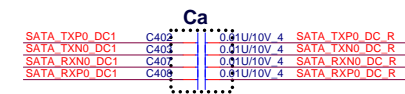
SATA Re-driver

Ra & Rb need place close

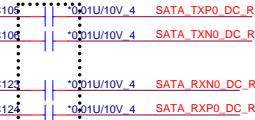
HOST



DEVICE

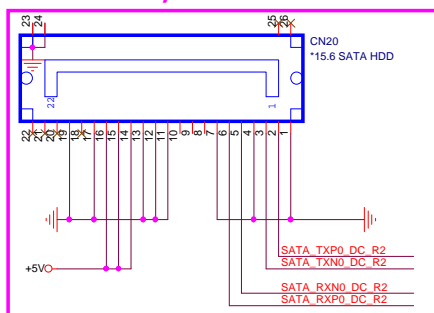


Cb

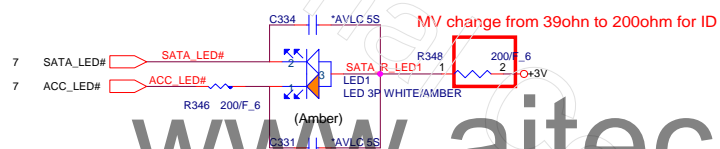


footprint check OK

SI-co-lay SATA HDD Connector



SATA LED



MV change from 39ohm to 200ohm for ID

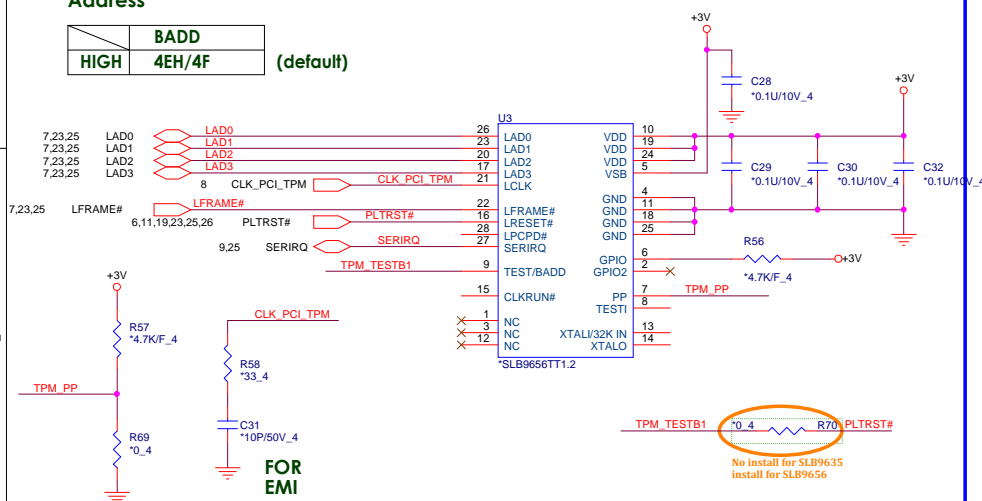
SATA re-driver IC
stuff Rb,Cb , unstuff Ra,Ca
unstuff SATA re-driver IC
stuff Ra,Ca , unstuff Rb,Cb

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TPM (1.2)

Address

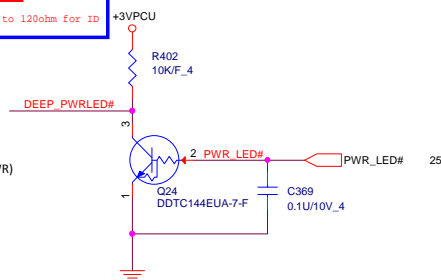
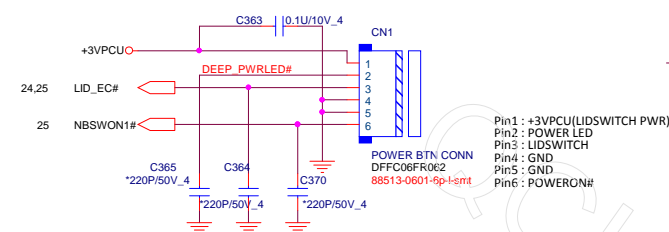
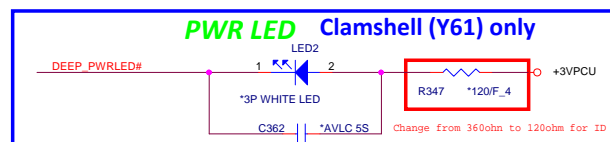
	BADD
HIGH	4EH/4F (default)



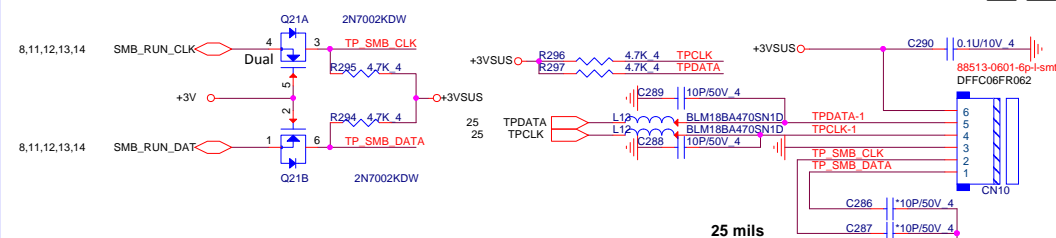
6,7,8,9,10,11,12,13,14,15,16,17,18,19,22,23,24,25,26,31,32 +3V
16,17,18,22,23,32 +5V
4,7,22,23,25,27,28 +3VPCU
27 BATT+

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	Quanta Computer Inc.	
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	HDD/mSATA/FAN/LED	
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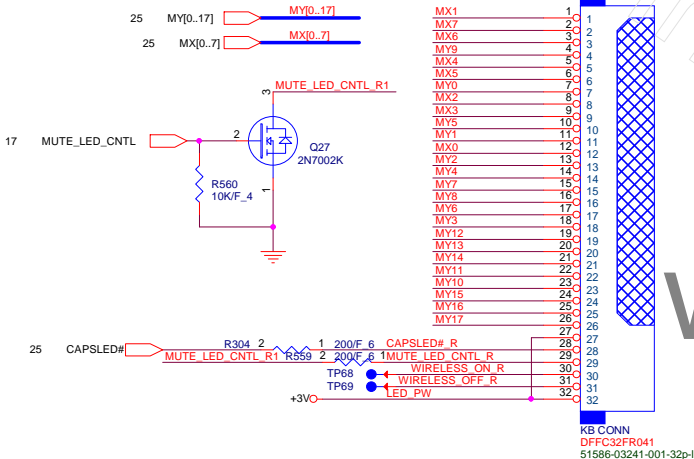
Power Botton Connector



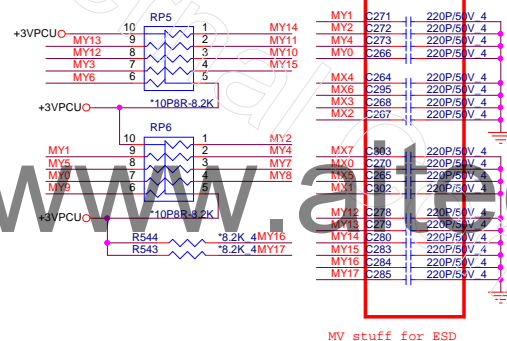
Touch Pad Connector



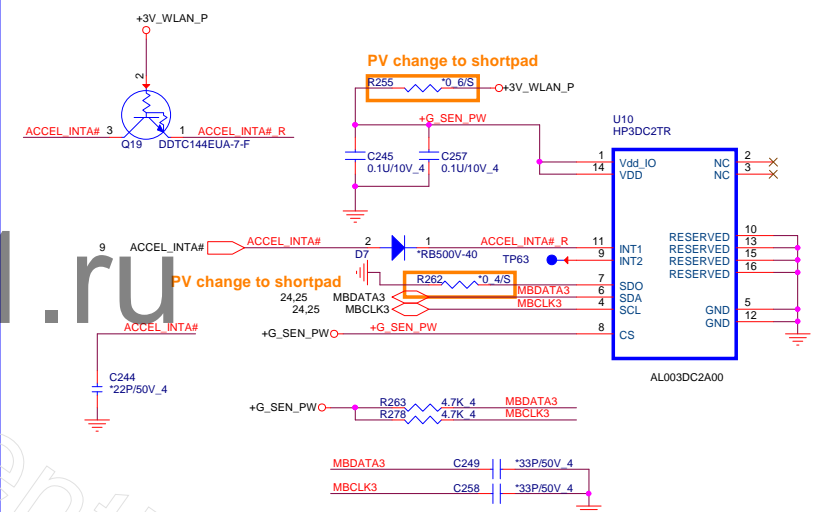
KEYBOARD Con.



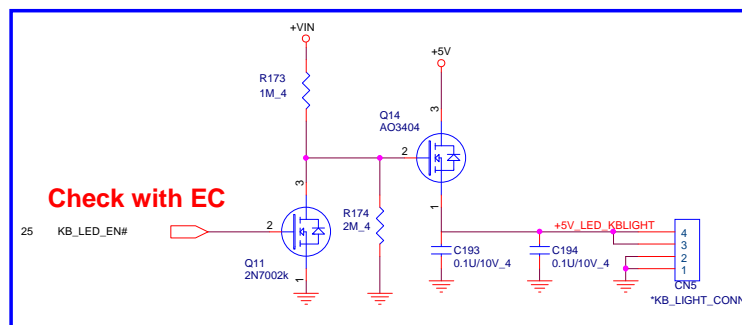
KEYBOARD PULL-UP



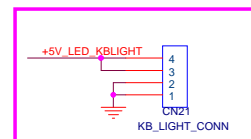
Accelerometer Sensor



15" KB backlight only



Co-lay





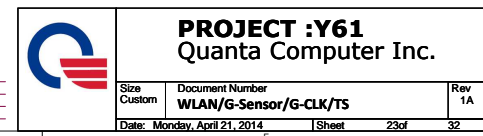
The diagram illustrates a PCB layout with various components and their connections. The components are labeled as follows:

- H4: *h-c315i158d118p2
- H1: *h-c315i158d118p2
- H12: *h-c315i158d118p2
- H7: *H-TC315BC276i158D118P2
- H11: *h-c315i158d118p2
- H10: *h-c315i158d118p2
- H9: *h-c315i158d118p2
- H3: *O-V61-1
- H13: *H-C79D79N
- H6: *H-C79D79N
- H8: *H-O102X79D102X79N
- H5: *intel-bkt-shark-ult
- SPAD1: *SPAD-C315
- SPAD2: *SPAD-C315
- SPAD3: *spad-re1303x79
- H14: *h-c315i158d118p2

The layout includes ESD protection components and connections:

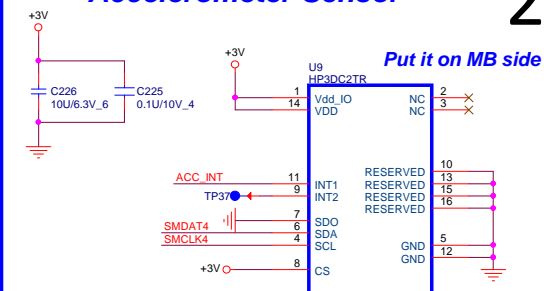
- ESD_GND: Ground connection for ESD protection.
- C515, C516, C517, C518: Capacitors used for ESD protection.
- *Clamp-Diode: Diodes used for ESD protection.
- PV add for ESD: A magenta-colored section indicating a voltage addition for ESD protection.
- MV add for ESD: A red-colored section indicating a voltage addition for ESD protection.

6,7,8,9,10,11,12,13,14,15,16,17,18,19,21,22,24,25,26,31,32 +PRWSRC
16,17,18,21,22,32 +3V
4,7,22,25,27,28 +5V
+3VPCU

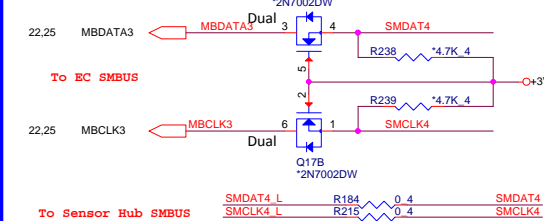


Accelerometer Sensor

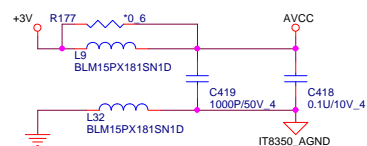
Put it on MB side



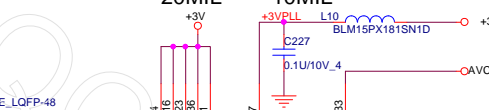
Close to U9



Note: Place all capacitors close to IT8350.



20MIL 10MIL (For PLL Power)



To APU 9 ACCEL_INTH# R488 *0.4 ACC_INT

Reserved SMBus channel 0 for debugging & updating FW
Reserved
SMBus channel 4 for connecting the Sensor (G-sensor)

IT8350E
LQFP-48

Reserved TX/RX for debugging

if no use ADC function,
please pull down to GND
SMINTx for sensor interrupt

GPG2 can't floating

For Home button IC update fw
GPG2 Pull High Enable mirror function.
GPG2 Pull Low Disable mirror function.

3 IN 1-Sensor
connector to HOME IC

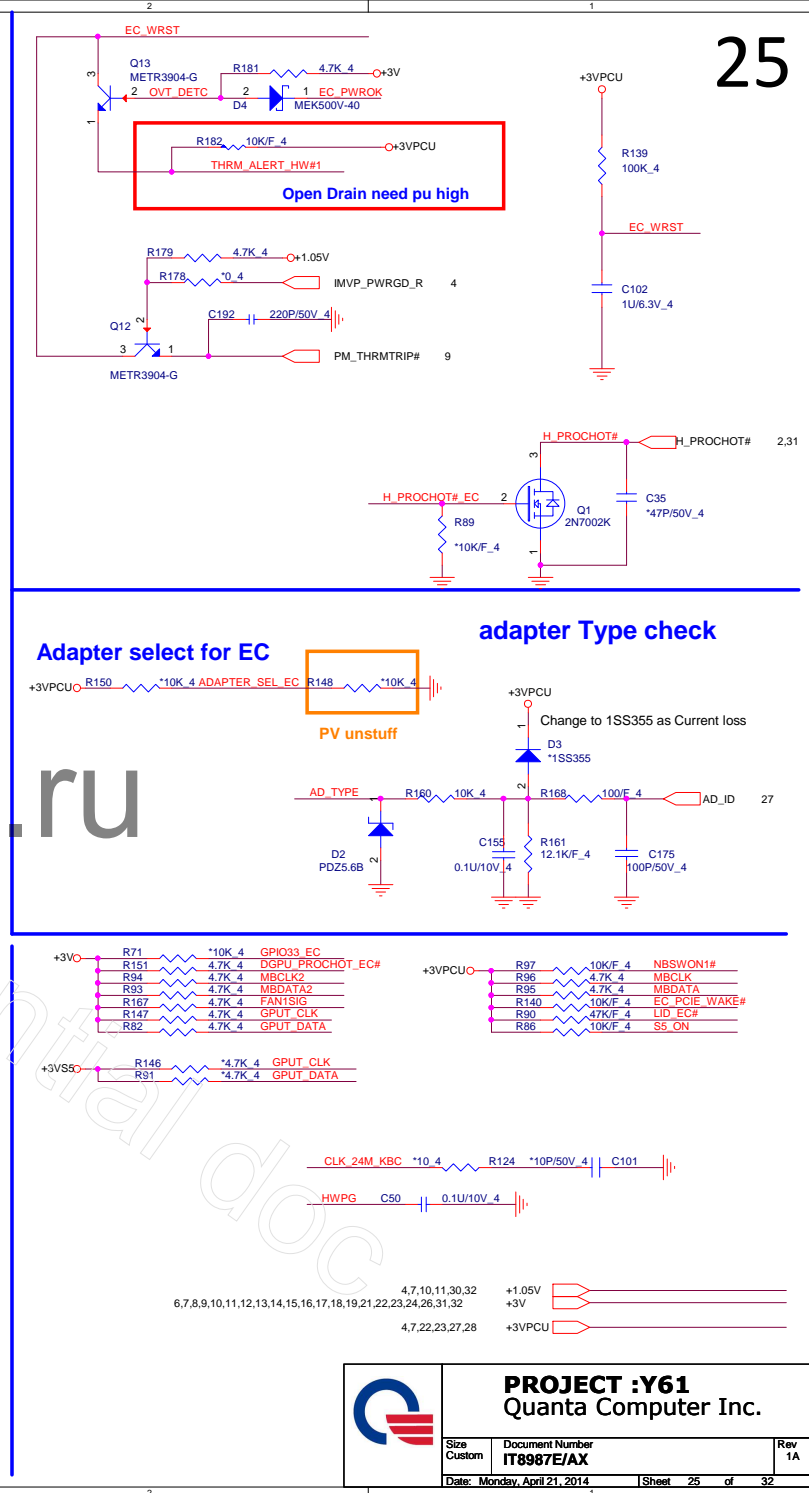
SI co-lay 6 pin TS CON

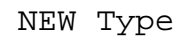
External crystal is must be item
when USB func. is used !

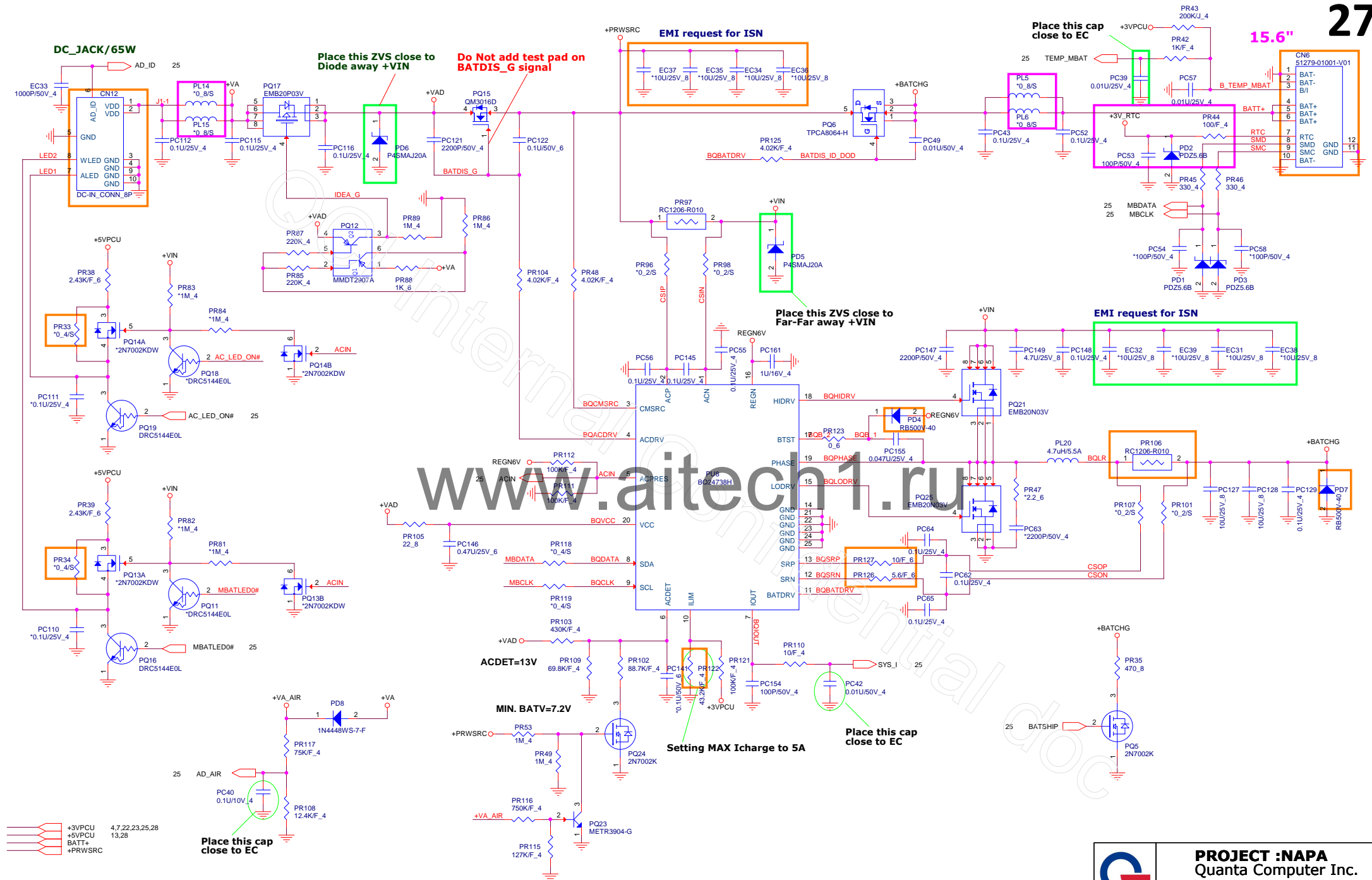
32.768kHz clock lines:

- If possible, please avoid using any through-hole.
- Please make the trace length short, and the trace width wide enough.
- The spacing to the closest neighbor should be wide enough.

PROJECT :Y61 Quanta Computer Inc.		
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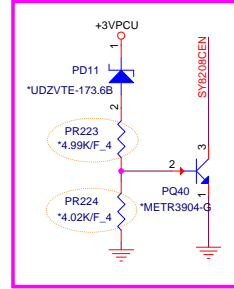
SI reserve for EMI



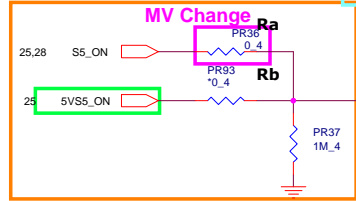
+3VS5 6,7,9,10,20,23,24,25,30,32
+5VS5 13,18,20,29,30,31,32

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

MV Change



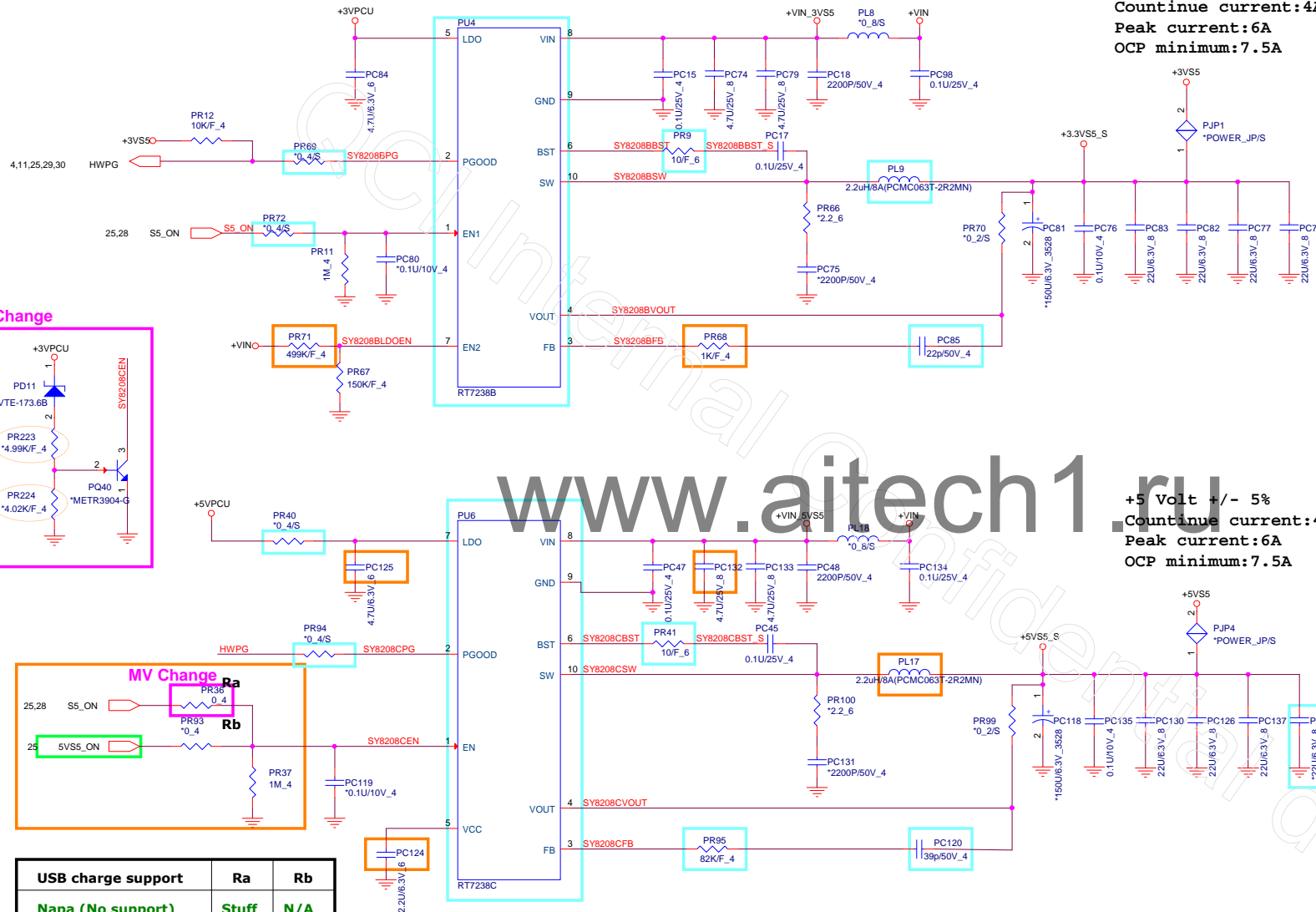
MV Change



USB charge support	Ra	Rb
Napa (No support)	Stuff	N/A
Whisky (Support)	N/A	Stuff

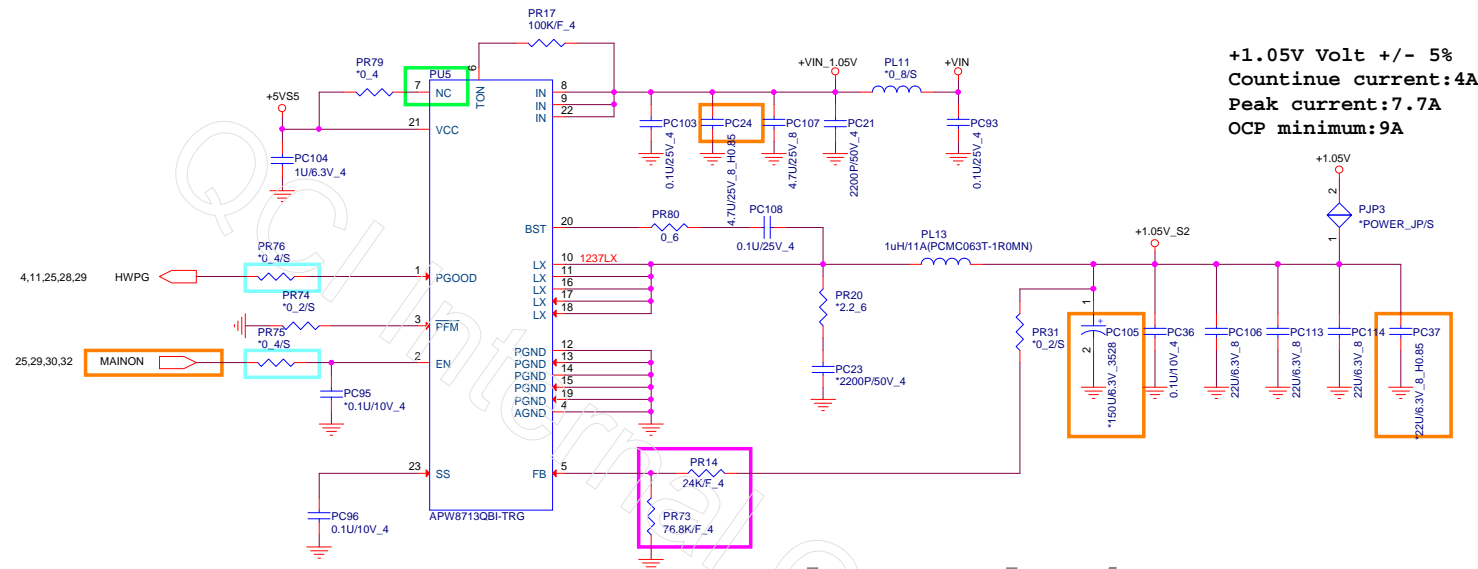
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+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

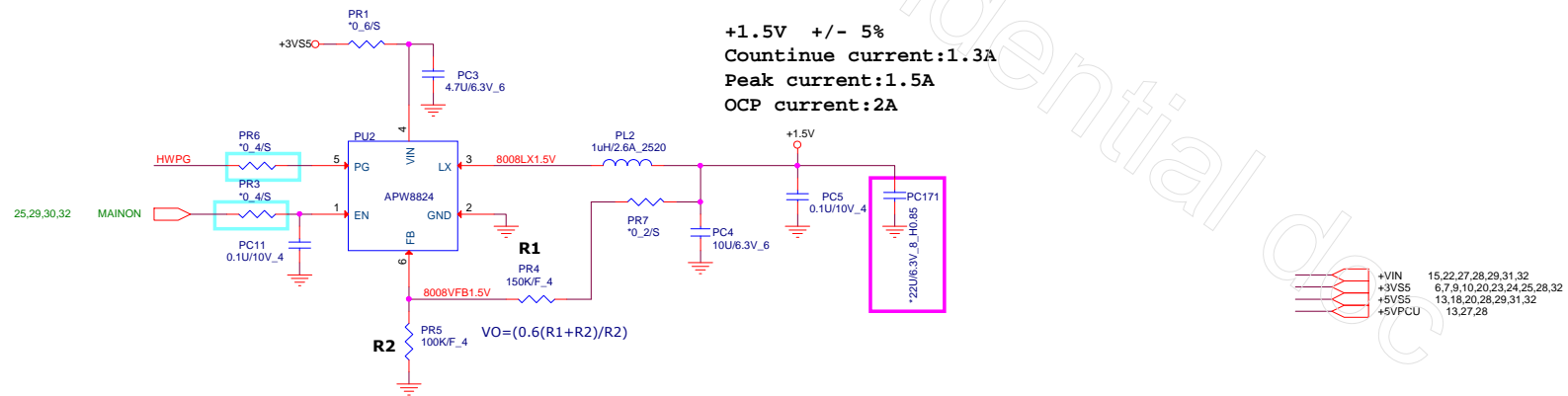


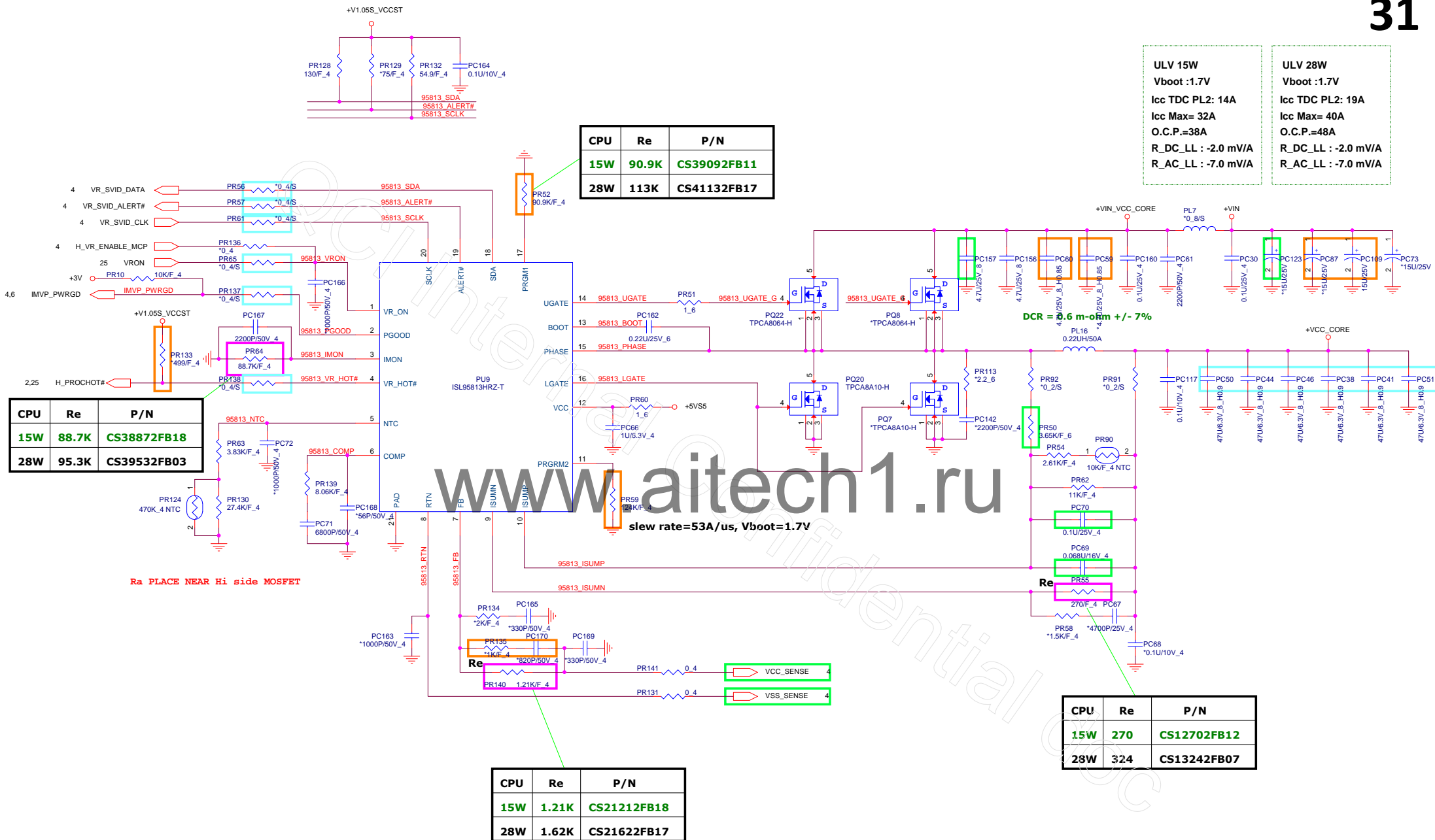
PROJECT :NAPA
Quanta Computer Inc.

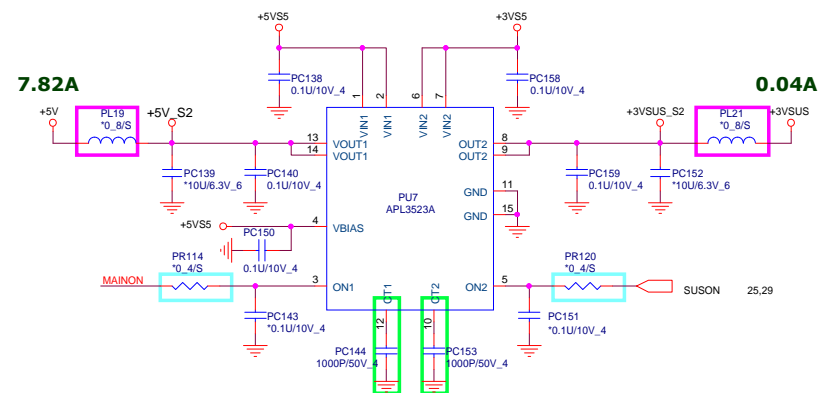
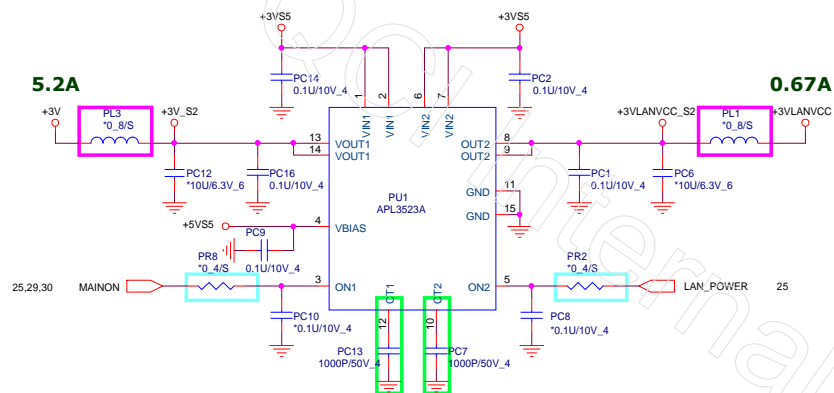
Size Custom Document Number 3/5VS5 (SY8208B/SY8208C) Rev 1A
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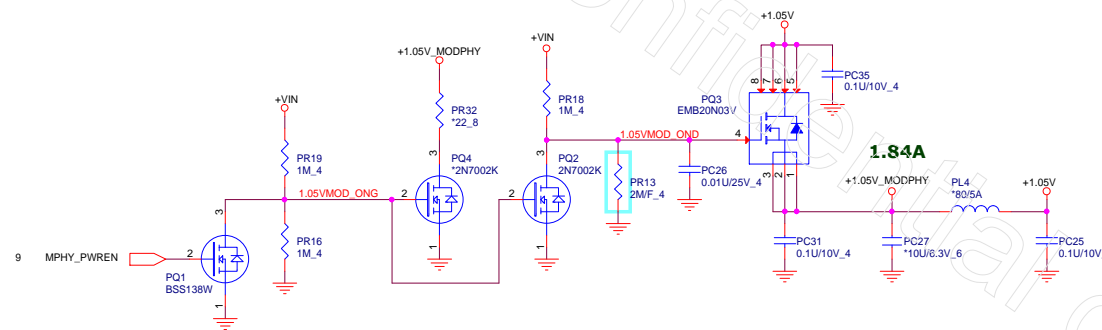
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6,7,8,9,10,11,12,13,14,15,16,17,18,19,21,22,23,24,25,26,31	+3V
16,17,18,21,22,23	+5V
15,22,27,28,29,30,31	+VIN
6,7,8,10,20,23,24,25,28,30	+3VSS
13,18,20,28,29,30,31	+5VSS
19	+3VLANVCC